

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Gattiker et al.

DOCKET NO: AUS920030654US1

SERIAL NO.: 10/728,172

FILE DATE: 12-03-2003

TITLE OF APPL.: METHOD AND SYSTEM FOR DEFECT EVALUATION USING  
QUIESCENT POWER PLANE CURRENT (IDDQ) VOLTAGE  
LINEARITY

Mail Stop Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Weiss, Moy & Harris, P.C.  
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Scottsdale, AZ 85251-3989

**INFORMATION DISCLOSURE STATEMENT**

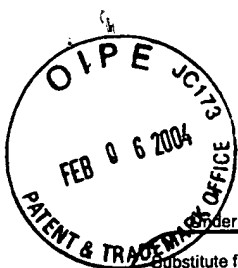
Dear Sir:

This information Disclosure Statement is submitted in regards to the above-identified patent application. A PTO-SB/08 form is attached along with copies of the references cited therein.

No fee is believed to be required in connection with this Information Disclosure Statement. However, if there is any fees incurred by this transmittal, please deduct them from IBM Deposit Account No. 09-0447.

Respectfully submitted,

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		<b>Complete if Known</b>			
		Application Number	10/728,172		
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		First Named Inventor	Gattiker et al.		
		Art Unit			
		Examiner Name			
Sheet	1	of	3	Attorney Docket Number	AUS920030654US1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		JONATHAN T-Y CHANG & EDWARD J. McCLUSKEY Quantitative Analysis of Very-Low-Voltage Testing, 1996	
		JONATHAN T-Y CHANG, CHAO-WEN TSENG, YI-CHIN, SANJAY WATTAL, MIKE PURTELL AND EDWARD McCLUSKEY Experiemental results for IDDQ and VLV Testing	
		R. RODRIGUIZ-MONTANES, J. FIGUERIAS Bridges in Sequential CMOS Clrcuits: Current-Voltage Signature, 1997	
		R. RODRIGUIZ-MONTANES, J. FIGUERIAS IDDQ-VDD Signatures for CMOS Circuits with Bridging Defects, 1996	
		R. RODRIGUIZ-MONTANES, J. FIGUERIAS Bridges in Sequential CMOS Clrcuits: Current-Voltage Signature, 1997	
		ANNE GATTIKER, PHIL NIGH, AND THOMAS VOGELS IC Testing: Background, Directions and Opportunities for Failure Analysis	
		HONG HAO AND EDWARD J. McCLUSKEY "Resistive Shorts" within CMOS Gates, 1991	
		HONG HAO AND EDWARD J. McCLUSKEY Very-Low-Voltage Testing for Weak CMOS Logic ICs, 1993	
		HONG HAO AND EDWARD J. McCLUSKEY Analysis of Gate Oxide Shorts in CMOS Circuits, 1993	
		CHARLES F. HAWKINS AND JERRY M. SODEN Electrical Failure Mode Characterization in CMOS ICs	

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		JERRY M. SODEN, CHARLES F. HAWKINS & ANTHONY C. MILLER Identifying defects in deep-submicron CMOS ICs, 1996	
		JERRY M. SODEN, CHARLES F. HAWKINS, RONALD R. FRITZEMEIER & LUTHER K. HORNING Quiescent Power Supply Current Measurement for CMOs IC Defect Detection, 1989	
		DOUG JOSEPHSON, MARK STOREY, DAN DIXON, HEWLETT-PACKARD Microprocessor IDDQ Testing: A Case Study, 1995	
		ALI KESHAVARZI, KAUSHIK ROY, MANOJ SACHDEV, CHARLES F. HAWKINS, K. SOUMYANATH, VLVEK DE Multiple-Parameter CMOS IC Testing with Increased Sensitivity for IDDQ, 2000	
		BRAM KRUSEMAN, STEFAN van den OETELAAR, AND JOSEP RIUS Comparisons of IDDQ Testing and Very-Low Voltage Testing, 2002	
		BORIS LISENER AND YURI MITNICK Fault Model for VLSI Circuits Reliability Assessment, 1999	
		BORIS LISENER, DMITRY VEINGER AND YURI MITNICK Short High Voltage Stress for Design-to-Process Characterization, 1999	
		PHIL NIGH AND ANNE GATTIKER Test Method Evaluation Experiments & Data, 2000	
		PHIL NIGH, DAVE VALLETT, ATUL PATEL & JASON WRIGHT Failure Analysis of Timing and IDDQ-only Failures from the SEMATECH Test Methods Experiment, 1998	
		ALAN W. RIGHTER, CHARLES F. HAWKINS, JERRY M. SODEN, PETER MAXWELL CMOS IC Reliability Indicators and Burn-In Economics, 1998	

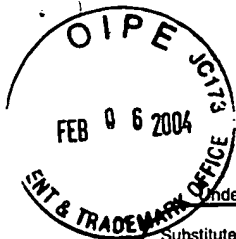
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**INFORMATION DISCLOSURE  
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Sheet 3

of 3

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		R. RODRIGUIZ-MONTANES, J.A. SEGURA, V.H.CHAMPAC, J. FIGUERAS, J.A. RUBIO Current vs. Logic Testing of Gate Oxide Short, Floating Gate and Bridging Failures in CMOS, 1991	
		MICHAEL RUBIN, DAVID LEARY AND SAUL NATAN Yield Enhancement and Yield Management of Silicon Foundries Using IDDQ " Stress Current Signature", 2001	
		YASUO SATO, MASAKI KOHNO, TOSHIO IKEDA, IWAO YAMAZAKI, & MASATO HAMAMOTO An Evaluation of Defect-Oriented Test: WELL-controlled Low Voltage Test, 2001	
		CHAO-WEN TSENG, RAY CHEN, PHIL NIGH & EDWARD J. McCLUSKEY MINVDD Testing for Weak CMOS ICs, 2001	
		T.J. VOGELS Effectiveness of I-V Testing in Comparison to IDDQ Tests, 2003	

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